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# **VIPA System 300S**



SPEED7 - CP | 341-2CH71 | Manual

HB140E\_CP | RE\_341-2CH71 | Rev. 09/46 November 2009



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VIPA GmbH, Ohmstraße 4, 91074 Herzogenaurach, Germany

Telefax:+49 9132 744 1204 EMail: documentation@vipa.de

#### **Technical support**

Contact your local VIPA Customer Service Organization representative if you encounter problems with the product or have questions regarding the product. If you are unable to locate a customer service center, contact VIPA as follows:

VIPA GmbH, Ohmstraße 4, 91074 Herzogenaurach, Germany

Telephone: +49 9132 744 1150/1180 (Hotline) EMail: support@vipa.de

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# About this manual

This manual describes the CP 341S with double RS422/485 interface of the System 300S from VIPA. Here you may find every information for commissioning and operation.

Overview Chapter 1: Basics This Basics contain hints for the usage and information about a SPEED7 system from VIPA. General information about the System 300S like dimensions and

## Chapter 2: Assembly and installation guidelines

In this chapter you will find all information, required for the installation and the cabling of a PLC with the components of the System 300.

## Chapter 3: Hardware description

environment conditions will also be found.

Here the hardware components of the CP 341S are more described. The technical data are to be found at the end of the chapter.

## Chapter 4: Deployment

Contents of this chapter is the hardware configuration and the parameterization of the CP. In addition the communication between CPU and CP 341S by means of function blocks is described.

## Chapter 5: Communication protocols

In this chapter the communication protocols are described, which are supported by the CP. Here you may find the protocol specific parameters and if necessary the functionality of the corresponding protocol.

## Chapter 6: Diagnostics and error behavior

In this chapter the possibilities of diagnostics and the error behavior of the CP is more described. Each CP part has its own diagnostics buffer for about 100 diagnostics entries and these are accessible as record sets. The record set of the corresponding CP part may be accessed by means of

the SFC 59 RD\_REC.

The manual describes the CP 341S with double RS422/485 interface from **Objective and** VIPA. It contains a description of the construction, project implementation contents and usage. This manual is part of the documentation package with order number HB140E\_CP and relevant for: Product Order number as of state: CP HW CP FW CP 341S-2RS422/485 VIPA 341-2CH71 01 V100 The manual is targeted at users who have a background in automation **Target audience** technology. Structure of the The manual consists of chapters. Every chapter provides a self-contained description of a specific topic. manual Guide to the The following guides are available in the manual: document an overall table of contents at the beginning of the manual an overview of the topics for every chapter an index at the end of the manual. **Availability** The manual is available in: printed form, on paper • in electronic form as PDF-file (Adobe Acrobat Reader) Important passages in the text are highlighted by following icons and Icons Headings headings: Danger! Immediate or likely danger. Personal injury is possible. Attention! Damages to property is likely if these warnings are not heeded. Note! Supplementary information and useful tips.

# **Safety information**

Applications conforming with specifications The CP is constructed and produced for:

- for the deployment with VIPA SPEED-Bus
- communication and process control
- general control and automation applications
- industrial applications
- operation within the environmental conditions specified in the technical data
- installation into a cubicle



## Danger!

This device is not certified for applications in

• in explosive environments (EX-zone)

Documentation

The manual must be available to all personnel in the

- project design department
- installation department
- commissioning
- operation



# The following conditions must be met before using or commissioning the components described in this manual:

- Modification to the process control system should only be carried out when the system has been disconnected from power!
- Installation and modifications only by properly trained personnel
- The national rules and regulations of the respective country must be satisfied (installation, safety, EMC ...)

Disposal

National rules and regulations apply to the disposal of the unit!

# Chapter 1 Basics

OverviewThis Basics contain hints for the usage and information about a SPEED7<br/>system from VIPA.General information about the System 300S like dimensions and<br/>environment conditions will also be found.

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# Safety Information for Users

Handling of electrostatic sensitive modules VIPA modules make use of highly integrated components in MOS-Technology. These components are extremely sensitive to over-voltages that can occur during electrostatic discharges.

The following symbol is attached to modules that can be destroyed by electrostatic discharges.



The Symbol is located on the module, the module rack or on packing material and it indicates the presence of electrostatic sensitive equipment.

It is possible that electrostatic sensitive equipment is destroyed by energies and voltages that are far less than the human threshold of perception. These voltages can occur where persons do not discharge themselves before handling electrostatic sensitive modules and they can damage components thereby, causing the module to become inoperable or unusable.

Modules that have been damaged by electrostatic discharges can fail after a temperature change, mechanical shock or changes in the electrical load.

Only the consequent implementation of protection devices and meticulous attention to the applicable rules and regulations for handling the respective equipment can prevent failures of electrostatic sensitive modules.

Modules must be shipped in the original packing material.

modules Measurements and

sensitive modules

alterations on

electrostatic

Shipping of

When you are conducting measurements on electrostatic sensitive modules you should take the following precautions:

- Floating instruments must be discharged before use.
- Instruments must be grounded.

Modifying electrostatic sensitive modules you should only use soldering irons with grounded tips.



## Attention!

Personnel and instruments should be grounded when working on electrostatic sensitive modules.

System 300S

# **General description of the System 300**

The System 300The System 300 is a modular automation system for middle and high<br/>performance needs, which you can use either centralized or decentralized.<br/>The single modules are directly clipped to the profile rail and are connected<br/>together with the help of bus clips at the backside.<br/>The CPUs of the System 300 are instruction set compatible to S7-300 from<br/>Siemens.

System 300V VIPA differentiates between System 300V and System 300S.

System 300V

The System 300V allows you to resolve automation tasks centralized and decentralized. The single modules of the System 300V from VIPA are similar in construction to Siemens. Due to the compatible backplane bus, the modules from VIPA and Siemens can be mixed.

• System 300S

The System 300S extends the central area with high-speed CPUs that have the integrated SPEED7 chip. Additionally some CPU's have got a parallel SPEED-Bus that allows the modular connection of fast peripheral modules like IOs or bus master.



# System 300S

**Overview** 

The CPUs 31xS are based upon the SPEED7 technology. This supports the CPU at programming and communication by means of co-processors that causes a power improvement for highest needs.

Except of the basic variant, all SPEED7-CPUs are provided with a parallel SPEED-Bus that enables the additional connection of up to 10 modules from the SPEED-Bus periphery. While the standard peripheral modules are plugged-in at the right side of the CPU, the SPEED bus peripheral modules are connected via a SPEED-Bus bus connector at the left side of the CPU.



**CPU 31xS** The System 300S series consists of a number of CPUs. These are programmed in STEP<sup>®</sup>7 from Siemens. For this you may use WinPLC7 from VIPA or the Siemens SIMATIC manager.

CPUs with integrated Ethernet interfaces or additional serial interfaces simplify the integration of the CPU into an existing network or the connection of additional peripheral equipment.

The user application is stored in the battery buffered RAM or on an additionally pluggable MMC storage module.

Due to the automatic address allocation, the deployment of the CPUs 31xS allows to address 32 peripheral modules.

Additionally some SPEED7-CPUs have got a parallel SPEED-Bus that allows the modular connection of fast peripheral modules like IOs or bus master.

SPEED-Bus	The SPEED-Bus is a 32Bit parallel bus developed from VIPA with a maximum data rate of 40MByte/s. Via the SPEED-Bus you may connect up to 10 SPEED-Bus modules to your CPU 31xS. In opposite to the "standard" backplane bus where the modules are plugged-in at the right side of the CPU by means of single bus connectors, the modules at the SPEED-Bus are plugged-in at the left side of the CPU via a special SPEED-Bus rail. VIPA delivers profile rails with integrated SPEED-Bus for 2, 6 or 10 SPEED-Bus peripheral modules with different lengths.
SPEED-Bus peripheral modules	<ul> <li>The SPEED-Bus peripheral modules may exclusively plugged at the SPEED-Bus slots at the left side of the CPU. The following SPEED-Bus modules are in preparation:</li> <li>Fast fieldbus modules like Profibus DP, Interbus, CANopen master and CANopen slave</li> <li>Fast CP 343 (CP 343 Communication processor for Ethernet)</li> <li>Fast CP 341 with double RS 422/485 interface</li> <li>Fast digital input-/output modules (Fast Digital IN/OUT)</li> </ul>
Memory management	Every CPU 31xS has an integrated work memory. During program run the total memory is divided into 50% for program code and 50% for data. Starting with CPU firmware 3.0.0 there is the possibility to extend the total memory to its maximum by means of a MCC memory extension card.
Integrated Profibus DP master	The CPUs of the System 300S series with SPEED-Bus have an integrated Profibus DP master. Via the DP master with a data range of 1kByte for in- and output you may address up to 124 DP slaves. The project engineering takes place in WinPLC7 from VIPA or in the hardware configurator from Siemens.
Integrated Ethernet PG/OP channel	Every CPU 31xS has an Ethernet interface for PG/OP communication. Via the "PLC" functions you may directly access the Ethernet PG/OP channel and program res. remote control your CPU. A max. of 2 PG/OP connections is available. You may also access the CPU with a visualization software via these connections.

Operation Security	<ul> <li>Wiring by means of spring pressure connections (CageClamps) at the front connector</li> </ul>		
	Core cross-section 0.082.5mm <sup>2</sup>		
	I otal isolation of the wiring at module change		
	Potential separation of all modules to the backplane bus		
	• ESD/Burst acc. IEC 61000-4-2/IEC 61000-4-4 (up to level 3)		
	<ul> <li>Shock resistance acc. IEC 60068-2-6 / IEC 60068-2-27 (1G/12G)</li> </ul>		
Environmental	<ul> <li>Operating temperature: 0 +60°C</li> </ul>		
conditions	<ul> <li>Storage temperature: -25 +70°C</li> </ul>		
	<ul> <li>Relative humidity: 5 95% without condensation</li> </ul>		
	<ul> <li>Ventilation by means of a fan is not required</li> </ul>		
Dimensions/	• Available lengths of the profile rail in mm: 160, 482, 530, 830 and 2000		
Weight	Dimensions of the basic enclosure:		
	1tier width: (HxWxD) in mm: 40x125x120		
	2tier width: (HxWxD) in mm: 80x125x120		
Compatibility	Modules and CPUs of the System 300 from VIPA and Siemens may be used at the "Standard" bus as a mixed configuration.		
	The project engineering takes place in WinPLC7 from VIPA or in the hardware configurator from Siemens.		
	The SPEED7 CPUs from VIPA are instruction compatible to the programming language STEP <sup>®</sup> 7 from Siemens and may be programmed via WinPLC7 from VIPA or via the Siemens SIMATIC manager.		
	Here the instruction set of the S7-400 from Siemens is used.		
	Note!		
1	Please do always use the <b>CPU 318-2DP (6ES7 318-2AJ00-0AB0/V3.0)</b> from Siemens of the hardware catalog to project a SPEED7-CPU with SPEED-Bus from VIPA. For the project engineering, a thorough knowledge of the Siemens SIMATIC manager and the hardware configurator from Siemens is required!		
Integrated power supply	Every CPU res. bus coupler comes with an integrated power supply. The power supply has to be supplied with DC 24V. By means of the supply voltage, the bus coupler electronic is supplied as well as the connected modules via backplane bus. Please regard that the integrated power supply may supply the backplane bus the backplane bus (SPEED-Bus and Standard-Bus) depending on the CPU with a sum with max. 5A. The power supply is protected against inverse polarity and overcurrent.		
	Every SPEED-Bus rail has a plug-in option for an external power supply. This allows you to raise the maximum current at the backplane bus for 5.5A.		

# Chapter 2 Assembly and installation guidelines

**Overview** In this chapter you will find all information, required for the installation and the cabling of a process control with the components of the System 300.

#### 

# **Overview**

General While the standard peripheral modules are plugged-in at the right side of the CPU, the SPEED-Bus peripheral modules are connected via a SPEED-Bus bus connector at the left side of the CPU.

> VIPA delivers profile rails with integrated SPEED-Bus for 2, 6 or 10 SPEED-Bus peripheral modules with different lengths.



Serial The single modules are directly installed on a profile rail and connected via the backplane bus coupler. Before installing the modules you have to clip Standard bus the backplane bus coupler to the module from the backside. The backplane bus coupler is included in the delivery of the peripheral modules.

Parallel With SPEED-Bus the bus connection happens via a SPEED-Bus rail integrated in the profile rail at the left side of the CPU. Due to the parallel SPEED-Bus SPEED-Bus not all slots must be occupied in sequence.

SLOT 1 for additional At SLOT 1 DCDC) you may plug either a SPEED-Bus module or an additional power supply.

Assembly possibilities

power supply

You may assemble the System 300 horizontally, vertically or lying.





embly	
0	



Please regard the allowed environment temperatures:

- horizontal assembly: from 0 to 60°C
- vertical assembly: from 0 to 40°C
- lying assembly: from 0 to 40°C

# Installation dimensions



# **Installation Standard-Bus**

## Approach

If you do not deploy SPEED-Bus modules, the assembly at the standard bus happens at the right side of the CPU with the following approach:



- Bolt the profile rail with the background (screw size: M6), so that you still have minimum 65mm space above and 40mm below the profile rail.
- If the background is a grounded metal or device plate, please look for a low-impedance connection between profile rail and background.
- Connect the profile rail with the protected earth conductor. For this purpose there is a bolt with M6-thread.
- The minimum cross-section of the cable to the protected earth conductor has to be 10mm<sup>2</sup>.



- Stick the power supply to the profile rail and pull it to the left side up to 5mm to the grounding bolt of the profile rail.
- Take a bus coupler and click it at the CPU from behind like shown in the picture.
- Stick the CPU to the profile rail right from the power supply and pull it to the power supply.
- Click the CPU downwards and bolt it like shown.
- Repeat this procedure with the peripheral modules, by clicking a backplane bus coupler, stick the module right from the modules you've already fixed, click it downwards and connect it with the backplane bus coupler of the last module and bolt it.





## Danger!

- Before installing or overhauling the System 300, the power supplies must be disconnected from voltage (pull the plug or remove the fuse)!
- Installation and modifications only by properly trained personnel!

# **Assembly SPEED-Bus**

## Pre-manufactured SPEED-Bus profile rail

For the deployment of SPEED-Bus modules, a pre-manufactured SPEED-Bus rail is required. This is available mounted on a profile rail with 2, 6 or 10 extension plug-in locations.



# Installation of the



- Bolt the profile rail with the background (screw size: M6), so that you still have minimum 65mm space above and 40mm below the profile rail.
- Please look for a low-impedance connection between profile rail and background



Connect the profile rail with the protected earth conductor.

The minimum cross-section of the cable to the protected earth conductor has to be  $10 \text{mm}^2$ .

## Profile rail



Order number	SPEED-	A	В	С
	Bus slots			
VIPA 390-1AB60	-	160mm	140mm	10mm
VIPA 390-1AE80	-	482mm	466mm	8,3mm
VIPA 390-1AF30	-	530mm	500mm	15mm
VIPA 390-1AJ30	-	830mm	800mm	15mm
VIPA 390-9BC00*	-	2000mm	-	15mm
VIPA 391-1AF10	2	530mm	500mm	15mm
VIPA 391-1AF30	6	530mm	500mm	15mm
VIPA 391-1AF50	10	530mm	500mm	15mm

\* Unit pack 10 pieces

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• Dismantle the according protection flaps of the SPEED-Bus plug-in locations with a screw driver (open and pull down).

For the SPEED-Bus is a parallel bus, not all SPEED-Bus plug-in locations must be used in series. Leave the protection flap installed at an unused SPEED-Bus plug-in location.

- At deployment of a DC 24V power supply, install it at the shown position at the profile rail at the left side of the SPEED-Bus and push it to the left to the isolation bolt of the profile rail.
- Fix the power supply by screwing.
- To connect the SPEED-Bus modules, plug it between the triangular positioning helps to a plug-in location marked with "SLOT ..." and pull it down.
- Only the "SLOT1 DCDC" allows you to plug-in either a SPEED-Bus module or an additional power supply.
- Fix the modules by screwing.







- To deploy the SPEED7-CPU exclusively at the SPEED-Bus, plug it between the triangular positioning helps to the plug-in location marked with "CPU SPEED7" and pull it down.
- Fix the CPU by screwing.

Please regard that not all CPU 31xS may be deployed at the SPEED-Bus!

Installation CPU with Standard-Bus-Modules



- If also standard modules shall be plugged, take a bus coupler and click it at the CPU from behind like shown in the picture.
- Plug the CPU between the triangular positioning helps to the plug-in location marked with "CPU SPEED7" and pull it down.
  - Fix the CPU by screwing.

Installation Standard-Bus-Modules



• Repeat this procedure with the peripheral modules, by clicking a backplane bus coupler, stick the module right from the modules you've already fixed, click it downwards and connect it with the backplane bus coupler of the last module and bolt it.



## Danger!

1 Nm

- Before installing or overhauling the System 300V, the power supplies must be disconnected from voltage (pull the plug or remove the fuse)!
- Installation and modifications only by properly trained personnel!

# Cabling

Overview

The power supplies and CPUs are exclusively delivered with CageClamp contacts. For the signal modules the front connectors are available from VIPA with screw contacts. In the following all connecting types of the power supplies, CPUs and input/output modules are described.



## Danger!

- Before installation or overhauling, the power supplies must be disconnected from voltage (pull the plug or remove the fuse)!
- Installation and modifications only by properly trained personnel!

### CageClamp technology (gray)

For the cabling of power supplies, bus couplers and parts of the CPU, gray connectors with CageClamp technology are used.

You may connect wires with a cross-section of 0.08mm<sup>2</sup> to 2.5mm<sup>2</sup>. You can use flexible wires without end case as well as stiff wires.



[1] Rectangular opening for screwdriver

[2] Round opening for wires

The picture on the left side shows the cabling step by step from top view.

- To conduct a wire you plug a fitting screwdriver obliquely into the rectangular opening like shown in the picture.
- To open the contact spring you have to push the screwdriver in the opposite direction and hold it.
- Insert the insulation striped wire into the round opening. You may use wires with a cross-section from 0.08mm<sup>2</sup> to 2.5mm<sup>2</sup>.
- By removing the screwdriver the wire is connected safely with the plug connector via a spring.

(3)

## CageClamp technology (green)

(1)

(2)

(3

For the cabling of e.g. the power supply of a CPU, green plugs with CageClamp technology are deployed.

Here also you may connect wires with a cross-section of 0.08mm<sup>2</sup> to 2.5mm<sup>2</sup>. You can use flexible wires without end case as well as stiff wires.



- [1] Test point for 2mm test tip
- [2] Locking (orange) for screwdriver
- [3] Round opening for wires

The picture on the left side shows the cabling step by step from top view.

- For cabling you push the locking vertical to the inside with a suiting screwdriver and hold the screwdriver in this position.
- Insert the insulation striped wire into the round opening. You may use wires with a cross-section from 0.08mm<sup>2</sup> to 2.5mm<sup>2</sup>.
- By removing the screwdriver the wire is connected safely with the plug connector via a spring.



## Note!

In opposite to the gray connection clamp from above, the green connection clamp is realized as plug that can be clipped off carefully even if it is still cabled.



Front connectors of the in-/output modules In the following the cabling of the three variants of the front-facing connector is shown:

For the I/O modules the following plugs are available at VIPA:



continued ...

- **20pole screw connection 40pole screw connection** VIPA 392-1AJ00 VIPA 392-1AM00 Push the release key at the front connector on Bolt the fixing screw of the front connector. the upper side of the module and at the same time push the front connector into the module until it locks. 2 TITLET TITLET 2 CITERING CONTRACTOR 0.4 ... 0.7 Nm Now the front connector is electrically connected with your module. Close the front flap. Fill out the labeling strip to mark the single channels and push the strip into the front flap.
- ... continue

# **Installation Guidelines**

General	The installation guidelines contain information about the interference free deployment of System 300 systems. There is the description of the ways, interference may occur in your control, how you can make sure the electromagnetic digestibility (EMC), and how you manage the isolation.
What means EMC?	Electromagnetic digestibility (EMC) means the ability of an electrical device, to function error free in an electromagnetic environment without being interferenced res. without interferencing the environment. All System 300 components are developed for the deployment in hard industrial environments and fulfill high demands on the EMC. Nevertheless you should project an EMC planning before installing the components and take conceivable interference causes into account.
Possible interference causes	<ul> <li>Electromagnetic interferences may interfere your control via different ways:</li> <li>Fields</li> <li>I/O signal conductors</li> <li>Bus system</li> <li>Current supply</li> <li>Protected earth conductor</li> </ul> Depending on the spreading medium (lead bound or lead free) and the distance to the interference cause, interferences to your control occur by means of different coupling mechanisms. One differs: <ul> <li>galvanic coupling</li> <li>capacitive coupling</li> <li>inductive coupling</li> <li>radiant coupling</li> </ul>

**Basic rules for** In the most times it is enough to take care of some elementary rules to guarantee the EMC. Please regard the following basic rules when installing your PLC.

- Take care of a correct area-wide grounding of the inactive metal parts when installing your components.
  - Install a central connection between the ground and the protected earth conductor system.
  - Connect all inactive metal extensive and impedance-low.
  - Please try not to use aluminum parts. Aluminum is easily oxidizing and is therefore less suitable for grounding.
- When cabling, take care of the correct line routing.
  - Organize your cabling in line groups (high voltage, current supply, signal and data lines).
  - Always lay your high voltage lines and signal res. data lines in separate channels or bundles.
  - Route the signal and data lines as near as possible beside ground areas (e.g. suspension bars, metal rails, tin cabinet).
- Proof the correct fixing of the lead isolation.
  - Data lines must be laid isolated.
  - Analog lines must be laid isolated. When transmitting signals with small amplitudes the one sided lying of the isolation may be favorable.
  - Lay the line isolation extensively on an isolation/protected earth conductor rail directly after the cabinet entry and fix the isolation with cable clamps.
  - Make sure that the isolation/protected earth conductor rail is connected impedance-low with the cabinet.
  - Use metallic or metalized plug cases for isolated data lines.
- In special use cases you should appoint special EMC actions.
  - Wire all inductivities with erase links that are not addressed by the System 300V modules.
  - For lightening cabinets you should prefer incandescent lamps and avoid luminescent lamps.
- Create an homogeneous reference potential and ground all electrical operating supplies when possible.
  - Please take care for the targeted employment of the grounding actions. The grounding of the PLC is a protection and functionality activity.
  - Connect installation parts and cabinets with the System 300V in star topology with the isolation/protected earth conductor system. So you avoid ground loops.
  - If potential differences between installation parts and cabinets occur, lay sufficiently dimensioned potential compensation lines.

Isolation of<br/>conductorsElectrical, magnetic and electromagnetic interference fields are weakened<br/>by means of an isolation, one talks of absorption.

Via the isolation rail, that is connected conductive with the rack, interference currents are shunt via cable isolation to the ground. Hereby you have to make sure, that the connection to the protected earth conductor is impedance-low, because otherwise the interference currents may appear as interference cause.

When isolating cables you have to regard the following:

- If possible, use only cables with isolation tangle.
- The hiding power of the isolation should be higher than 80%.
- Normally you should always lay the isolation of cables on both sides. Only by means of the both-sided connection of the isolation you achieve a high quality interference suppression in the higher frequency area.

Only as exception you may also lay the isolation one-sided. Then you only achieve the absorption of the lower frequencies. A one-sided isolation connection may be convenient, if:

- the conduction of a potential compensating line is not possible
- analog signals (some mV res. µA) are transferred
- foil isolations (static isolations) are used.
- With data lines always use metallic or metalized plugs for serial couplings. Fix the isolation of the data line at the plug rack. Do not lay the isolation on the PIN 1 of the plug bar!
- At stationary operation it is convenient to strip the insulated cable interruption free and lay it on the isolation/protected earth conductor line.
- To fix the isolation tangles use cable clamps out of metal. The clamps must clasp the isolation extensively and have well contact.
- Lay the isolation on an isolation rail directly after the entry of the cable in the cabinet. Lead the isolation further on to the System 300V module and **don't** lay it on there again!



## Please regard at installation!

At potential differences between the grounding points, there may be a compensation current via the isolation connected at both sides. Remedy: Potential compensation line

# Chapter 3 Hardware description

**Overview** Here the hardware components of the CP 341 are more described. The technical data are to be found at the end of the chapter.

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	Structure		
	Technical	data	

# **Properties**

**CP 341S-2RS422/485** 341-2CH71

- RS422/485 interface isolated to back plane bus
- The following protocols are supported:
  - ASCII - STX/ETX
- Parameterization via GSD file
- Up to 250 telegrams within the 1024byte sized receive and send buffer
- Baud rate parameterizable up to 115.2kbit/s
- Integrated diagnostics buffer each CP
- Power supply via back plane bus



### Order data

Туре	Order number	Description
CP 341S-2RS422/485	VIPA 341-2CH71	CP 341 with double RS422/485 interface
		Protocols: ASCII, STX/ETX

# Structure

CP 341S-2RS422/485 341-2CH71

VI	PA CP341S-2RS422/485	
	RUN	
۱Ħ	NTF	
∣⊟⊧	COM1	
⊟⊧	AULT1	
ı⊟ı	xD1	— 1
╽┢┍	RxD1	
▐┢╒	XTF2 COM2	
╽┢╒	AULT2	
IН	xD2	
F	RxD2	
VIP	A 341-2CH71 34	
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1		

[1] LED status indicators

The following components are under the front flap

- [2] RS422/485 COM1 interface
- [3] RS422/485 COM2 interface

## LEDs

The communication processor is provided with LEDs for the purpose of displaying the operating status. The following table shows the description and the color of these LEDs.

Name	Color	Description	
RUN	green	Blinks at start-up and firmware-update.	
		On at ready for communication	
INTF	red	On at an internal error of the module.	
		If this error just exists after PowerON,	
	L	please contact the VIPA hotline.	
EXTF1	red	On while wire break at COM1.	
FAULT1	red	On if COM1 is without parameters.	
		Blinks if COM1 has wrong parameters.	
		Flickers on parity error or character frame error	
	ļ		
TxD1	green	On if CP is sending user data via COM1	
RxD1	green	On if CP is receiving user data via COM1	
EXTF2	red	On while wire break at COM2.	
FAULT2	red	On if COM2 is without parameters.	
		Blinks if COM2 has wrong parameters.	
		Flickers on parity error or character frame error at COM2.	
TxD2	green	On if CP is sending user data via COM2.	
RxD2	green	On if CP is receiving user data via COM2.	

During firmware update at the corresponding CP the LEDs TxD and RxD Behavior on are on and the RUN-LED is blinking. The CPU LEDs show the termination firmware update of the firmware update.

Behavior on start-After PowerON every LED is on for a short time. Then only RUN is blinking. up As soon as the CP is ready for communication the RUN LED gets on. As soon as a communication processor is without parameters the corresponding FAULT LED is on.

**Power supply** The communication is power supplied via the back plane bus. The current consumption is max. 750mA.

#### RS422/485 interface

Logical conditions as voltage difference between 2 twisted lines

- Serial bus connection Full-duplex: Four-wire operation (RS422) Half-duplex: Two-wire operation (RS485)
- Data transfer rate up to 115.2kbit/s

## 9pin D-type jack



Pin	Designation	Input/ Output	Signal description
1	n.c.		
2	T(B)+	Output	Send data (four-wire)
3	R(B)+	Input	Receive data (four-wire)
	R(B)+/T(B)+	Input/Output	Receive/Send data (two-wire)
4	RTS	Output	Request to send: RTS "ON": CP ready to send RTS "OFF": CP is not sending
5	M5V (GND_ISO)	Output	Ground isolated
6	P5V (+5V_ISO)	Output	5V isolated
7	T(A)-	Output	Send data (four-wire)
8	R(A)-	Input	Receive data (four-wire)
	R(A)-/T(A)-	Input/Output	Receive/Send data (two-wire)
9	n.c.		



## Note!

Never connect the shield of the cable with GND\_ISO, as this could destroy the interface!

GND\_ISO must always be connected on both sides; otherwise the modules could be destroyed!

Isolated voltages P5V, M5V

RS485 cabling

RS422 cabling

Pin 6 (P5V) of the isolated interfaces carries the isolated 5V supply with the respective ground GND on pin 5 (M5V). You may use this isolated voltage to provide defined static voltage levels on the signaling lines by means of resistors and ensure that reflections are reduced to a minimum.



In the case of cables >50m you have to solder in a terminating resistor of approx. 330Ω on the receiver for data free traffic.



<sup>1)</sup> In the case of cables >50m you have to solder in a terminating resistor of approx.  $330\Omega$  on the receiver for data free traffic.

Defined static voltage levels by parameters For a connection with minimum reflections and the wire-break recognition at RS422/485 operation, the lines may be preset with defined static voltage levels.

At the CP interface the wiring of the receiver is realized as follows:

Value	Description	Wiring of the receiver
None	No preassignment of the receiving lines. This setting only makes sense with bus- capable special drivers.	R(B) + R(A) -
Signal R(A) 5Volt (Break evaluation) Signal R(B) 0Volt	With this preassignment break detection is possible at full-duplex operation (RS422).	0V R(B) + R(A) - 5V
Signal R(A) 0Volt Signal R(B) 5Volt	This preassignment corresponds to the idle state (no sender is activated) at half-duplex operation with RS485. Wire-break recognition is not possible, here.	5V R(B) + R(A) - 0V

# **Technical data**

## CP 341S-2RS422/485

Module name	VIPA 341-2CH71		
Dimensions and Weight			
Dimensions (WxHxD) in mm	40x125x120		
Weight	190g		
Electrical Data			
Voltage supply	5V via back plane bus		
Current consumption via back plane bus	max. 750mA		
Status monitor	via LED at the front side		
Power dissipation of the module	3.75W		
Protocols	ASCII, STX/ETX		
Plugs / Interfaces	double interface		
COM1/COM2	9pin D-type plug for RS422/485		
Isolation	to back plane bus		
Transfer distance	1200m at 19.2kbit/s		
	500m at 38.4kbit/s		
	250m at 76.8kbit/s		
Baud rate	max. 115.2kbit/s		
Interrupts			
Diagnostic interrupt	no		
Diagnostic functions			
Read-out diagnostic information	yes		
Environment conditions			
Operating temperature	060°C		
Transportation and storage temperature	-40°C to +70°C		
Relative humidity	max. 95% at +25°C		

# Chapter 4 Deployment

**Overview** Contents of this chapter is the hardware configuration and the parameterization of the CP. In addition the communication between CPU and CP 341S by means of function blocks is described.

Content	Торіс		Page
	Chapter 4	Deployment	
	Fast intro	duction	
	Hardware	configuration	4-4
	Communio	cation with the user program	
	Firmware	update	

# **Fast introduction**

# **Overview** The integration of the CP into your SPS system should take place with the following proceeding:

- Assembly and commissioning
- Hardware configuration (integration CP in CPU)
- Protocol parameters
- Communication with the user program

Assembly and commissioning

- Install your SPEED-Bus system with a SPEED7 CPU and a CP 341.
- Wire-up the system. A detailed description about this may be found in the chapter "Assembly and installation guidelines".
- Switch power ON. → After a short boot time the CP is in the system without any protocol.
- Start the Siemens SIMATIC manager with an online connection to the CPU. More about this may be found in the manual of the CPU.



## Note!

For the deployment of the System 300S modules at the SPEED-Bus you have to include the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA.

Hardware
configuration

- Install the SPEEDBUS.GSD from VIPA.
- For hardware configuration jump within your project to the hardware configurator of the Siemens SIMATIC manager.
- Insert a profile rail.
- Place the following Siemens CPU at slot 2: CPU 318-2DP (6ES7 318-2AJ00-0AB0/V3.0) and parameterize the CPU if necessary.
- If there are modules at the standard bus right beside the CPU and parameterize the modules if necessary.

The project engineering of the SPEED-Bus modules happens by means of a virtual Profibus DP master system. For this, place as last module a DP master (342-5DA02 V5.0) with master system.

- Now include for the CPU and <u>every</u> module at the SPEED-Bus a slave system "VIPA\_SPEEDBUS".
- Set as Profibus address the slot no. (100...110) of the module and place the according module from the hardware catalog of VIPA\_SPEEDBUS to slot 0 of the slave system.
- In this way place the SPEED-Bus CP 341-2CH71 according to your protocol. In the hardware catalog for each protocol at VIPA\_SPEEDBUS a CP 341-2CH71 is available.

Protocol	Via double-click open the properties of the CP. Here among others the
parameters	protocol parameters may be preset.

**Communication with the user program** For the processing of the connecting jobs at PLC side a user program is necessary in the CPU. Here the VIPA specific blocks FB 7 and FB 8 are used for communication between CPU, CP and a communication partner. These blocks may be found at www.vipa.de at *Downloads* > *VIPA LIB* as library for download.

By a cyclic call of these blocks data may be sent and received by the CP.

The conversion of the transfer protocols to the communication partner happens at the CP.

For each of these FBs an instance DB is necessary. This is to be indicated at the call of the corresponding FB. The data for communication are to be stored in each case in a send respectively receive DB.

To control the communication the FBs have control bits. Here the communication may be started, stopped or reset with the appropriate programming for the corresponding CP. There are status bits within the FBs for error evaluation.

These steps are more described in the following.

# Hardware configuration

**Preconditions** The hardware configurator is part of the Siemens SIMATIC manager. It serves the project engineering. The modules that may be configured here are listed in the hardware catalog.

For the deployment of the System 300S modules at the SPEED-Bus you have to include the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA.



### Note!

For the project engineering a thorough knowledge of the Siemens SIMATIC manager and the hardware configurator from Siemens is required!

# Include the SPEED7-GSD-file

The GSD (**G**eräte-**S**tamm-**D**atei) is online available in the following language versions. Further language versions are available on inquires.

Name	Language
SPEEDBUS.GSD	german (default)
SPEEDBUS.GSG	german
SPEEDBUS.GSE	english

The GSD files may be found at the service area of www.vipa.de.

The integration of the SPEEDBUS.GSD takes place with the following proceeding:

- Browse to www.vipa.de.
- Click to Service > Downloads > GSD files.
- Download the file *Cx000023\_Vxxx*.
- Extract the file to your work directory. The SPEEDBUS.GSD is stored in the directory *VIPA\_System\_300S*.
- Start the hardware configurator from Siemens.
- Close every project.
- Select **Options** > Install new GSD-file.
- Navigate to the directory *VIPA\_System\_300S* and select "SPEEDBUS.GSD".

The modules of the System 300S from VIPA are now included in the hardware catalog at *Profibus-DP / Additional field devices / I/O / VIPA\_SPEEDBUS*.

Steps of project engineering

The following text describes the approach of the project engineering of the CP 341 for SPEED-Bus in the hardware configurator from Siemens at an abstract sample.

The project engineering is separated into the following parts:

- Project engineering standard bus
- Project engineering SPEED-Bus as virtual Profibus network



Project engineering of the modules at the standard bus

- Start the hardware configurator from Siemens with a new project and insert a profile rail from the hardware catalog.
- Place the following Siemens CPU at slot 2: CPU 318-2DP (6ES7 318-2AJ00-0AB0/V3.0)
- Parameterize the CPU where appropriate. The parameter window opens by a double click on the according module.

If there are modules at the standard bus right beside the CPU, these are configured with the following approach:

- Include your System 300 modules at the standard bus in the plugged sequence starting with slot 4.
- Parameterize the modules where appropriate. The parameter window opens by a double click on the according module.
- Since as many as 32 modules may be addressed by the SPEED7 CPU in one row, but only 8 modules are supported by the Siemens SIMATIC manager, the IM 360 of the hardware catalog can be used as a virtual bus extension during project engineering. Here 3 further extension racks can be virtually connected via the IM 361. Bus extensions are always placed at slot 3.



Project engineering SPEED-Bus as virtual Profibus network The project engineering of the SPEED-Bus modules happens by means of a virtual Profibus DP master system. For this, place as last module a DP master (342-5DA02 V5.0) with master system.

For the deployment of the System 300S modules at the SPEED-Bus the inclusion of the System 300S modules into the hardware catalog via the GSD-file SPEEDBUS.GSD from VIPA is required.

After the installation of the SPEEDBUS.GSD you may locate at *Profibus DP / Additional field devices / I/O / VIPA\_SPEEDBUS* the DP slave system VIPA\_SPEEDBUS.

Now include for the CPU and <u>every</u> module at the SPEED-Bus a slave system "VIPA\_SPEEDBUS".

Set as Profibus address the slot no. (100...110) of the module and place the according module from the hardware catalog of VIPA\_SPEEDBUS to slot 0 of the slave system.

In this way place the SPEED-Bus CP 341-2CH71 according to your protocol. In the hardware catalog for each protocol at VIPA\_SPEEDBUS a CP 341-2CH71 is available.



The according module is to be taken over from the HW Catalog of VIPA\_SPEEDBUS to slot 0.

Properties CP 341-2CH71	The properties of the CP may be accessed by a double click at the CP, which corresponds to the protocol you want. Every parameter of the CP may be accessed by the registers <i>Address/ID</i> and <i>Parameter Assignment</i> .
Address/ID	
Output Input	By presetting a start address for the input respectively output area the beginning of the address area of the CPU may be determined, which is mapped by the module. Please regard that the base address for input and output are identical. Each interface occupies 16byte. The data of the COM2 interface are allocated with an offset of 16byte. The corresponding address value is necessary for integration in the user program. To access the COM2 interface you have to add 16 to the respective address value.
Process image	With the process image a consistent image of the process signal may be accessed during the program cycle. If the field <i>process image</i> shows the entry "" then the set address area is outside the process image. The entry "OB1-PA" indicates that the set address area is within the process image.
Parameter Assignment	Here the parameters, which correspond to the protocol, may be preset. More information concerning this may be found at chapter "Communication Protocols".

# Communication with the user program

**Overview** For the processing of the connecting jobs at PLC side a user program is necessary in the CPU. Here the following VIPA specific blocks are used for communication between CPU, CP and a communication partner:

Block	Symbol	Comment
FB 7	P_RCV_RK	Block for data receipt from a communication partner
FB 8	P_SND_RK	Block for data send to a communication partner

Installing blocks	The VIPA specific blocks may be found at www.vipa.de as downloadable library at the service area with <i>Downloads</i> > <i>VIPA LIB</i> . The library is available as packed zip-file. If you want to use VIPA specific blocks, you have to import the library into your project. Execute the following steps: • Extract FX000011_Vxxx.zip • "Retrieve" the library • Open library and transfer blocks into the project
Unzip FX000011_Vxxx.zip	Start your un-zip application with a double click on the file FX000011_Vxxx.zip and copy the file vipa.zip to your work directory. It is not necessary to extract this file, too.
Retrieve library	To retrieve your library for the SPEED7-CPUs, start the SIMATIC manager from Siemens. Open the dialog window for archive selection via <b>File</b> > <i>Retrieve</i> . Navigate to your work directory. Choose VIPA.ZIP and click at [Open]. Select a destination folder where the blocks are to be stored. [OK] starts the extraction.
Open library and transfer blocks to project	After the extraction open the library. Open your project and copy the necessary blocks from the library into the directory "blocks" of your project. Now you have access to the VIPA specific blocks via your user application.

Data consistencyThe data consistency is limited by the block size of 1024byte during<br/>communication between CPU and CP.For the consistent data communication of more than 1024byte the following<br/>is to be considered:<br/>FB8 - P\_SND\_RK:<br/>Access the send DB only again if the data were completely transferred<br/>(DONE = 1).FB7 - P\_RCV\_RK:<br/>Access the receive DB only again if the data were completely received<br/>(NDR = 1). After that the receive DB should be blocked (EN\_R = 0) as long<br/>as the data were treated.

**Communication principle** By a cyclic call of FB 7 and FB 8 data may be cyclic sent and received by the CP. On the CP the transmission of the communication protocols to the communication partner takes place, which may be configured by the hardware configuration. In the following these blocks are described.

**Receive data FB 7 - P\_RCV\_RK FB 7 - P\_RCV\_RK The FB 7 P\_RCV\_RK** transfers data from the CP to a data area of the CPU specified by the parameter *DB\_NO*, *DBB\_NO* and *LEN*. For data transfer the FB is to be called either cyclically or statically by a timer-driven program.

Information about the parameters, which were necessary for the loadable protocols may be found at the corresponding protocol description in the chapter "Communication protocols".

Parameter	Declaration	Data type	Description
EN_R	Input	BOOL	Enables data read
R	Input	BOOL	Aborts request - current request is aborted and receiving is
			blocked.
LADDR	Input	INT	Logical basic address of the CP - corresponds to the address of the hardware configuration of the CP.
DB_NO	Input	INT	Data block number - number of the receive DB, zero is not allowed.
DBB_NO	Input	INT	Data byte number - received data as of data byte
			$0 \leq \text{DBB}_NO \leq 8190$
L	Output	-	These parameters are not relevant for ASCII and 3964(R).
			But they may be used by loadable protocols.
NDR <sup>1)</sup>	Output	BOOL	Request complete without errors, data received
			Parameter STATUS = 00h
ERROR <sup>1)</sup>	Output	BOOL	Request complete with error
			Parameter STATUS contains error details
LEN <sup>1)</sup>	Output	INT	Length of the received telegram in byte
			$1 \leq \text{LEN} \leq 1024$
STATUS <sup>1)</sup>	Output	WORD	Specification of the error on ERROR = 1

## Parameter

<sup>1)</sup> Parameter is available until the next call of the FB.

**Release and** With the signal state "1" at parameter *EN\_R*, the software checks whether data can be read by the CP. A data transmission operation can run over cancel a request several program cycles, depending on the amount of data involved. An active transmission can be aborted with signal state "0" at the EN\_R parameter. The aborted receive request is terminated with an error message (STATUS). Receiving is deactivated as long as the EN R parameter shows the signal state "0". A running request may me canceled with R = "1" then the FB is reset to the basic state. Receiving is deactivated as long as the *R* parameter shows the signal state "1".

Startup	With every STOP-RUN transition the CP gets parameter data from the
synchronization	CPU. The CP accepts the parameters and waits for the ready for
	communication message of the CPU. The communication starts as soon
	as the CPU is ready for operation.

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#### Note!

A minimum pulse time is necessary for a signal change to be identified. Significant time periods are the CPU cycle time, the updating time on the CP and the response time of the communication partner.

Error indication The NDR output shows "request completed without errors/data accepted". If there was an ERROR, the corresponding event number is displayed in the STATUS. If no error occurs the value of STATUS is "0". NDR and ERROR/STATUS are also output in response to a RESET of the FB. In the event of an error, the binary result BR is reset. If the block is terminated without errors, the binary result has the status "1". Please regard the parameter NDR, ERROR and STATUS are only

available at one block call. For further evaluation these should be copied to a free data area.

Addressing With LADDR the address of the corresponding CP is specified. This is the address, which was specified during hardware configuration by means of the properties of the respective interface of the CP.

Please regard for each interface of the CP one address is used for input and output.

Data area The FB 7 - P RCV RK deals with an Instanz-DB I RCV RK. The DB no. is transmitted with the call.

It is not allowed to access the data of an instance DB.

Send data FB 8 - P_SND_RK	The FB 8 - P_SND_RK transfers a data block of a DB to the CP, specified by the parameters <i>DB_NO</i> , <i>DBB_NO</i> and <i>LEN</i> . For data transfer the FB is to be called either cyclically or statically by a timer-driven program.
	Information about the parameters, which were necessary for the loadable protocols, may be found at the corresponding protocol description in the chapter "Communication protocols".

### Parameter

Parameter	Declaration	Data type	Description
SF	Input	CHAR	S = Send, F = Fetch. At ASCII and 3964R the default
			value "S" for Send may be used
REQ	Input	BOOL	Initiates request with positive edge
R	Input	BOOL	Aborts request - current request is aborted and sending is
			blocked.
LADDR	Input	INT	Logical basic address of the CP - corresponds to the
			address of the hardware configuration of the CP.
DB_NO	Input	INT	Data block number - number of the send DB, zero is not
			allowed.
DBB_NO	Input	INT	Data byte number - transmitted data as of data byte
			$0 \leq \text{DBB}_NO \leq 8190$
LEN	Input	INT	Length of message frame to be sent in byte
			$1 \leq \text{LEN} \leq 1024$
R	Input	-	These parameters are not relevant for ASCII and 3964(R).
			But they may be used by loadable protocols.
DONE <sup>1)</sup>	Output	BOOL	Request complete without errors, data sent
			Parameter STATUS = 00h
ERROR <sup>1)</sup>	Output	BOOL	Request complete with error
			Parameter STATUS contains error details
STATUS <sup>1)</sup>	Output	WORD	Specification of the error on ERROR = 1

<sup>1)</sup> Parameter is available until the next call of the FB.

Release and T cancel a request

The data transmission is initiated by a positive edge at the *REQ* input of FB 8 - P\_SND\_RK. A data transmission operation can run over several program cycles, depending on the amount of data involved.

A running request may me canceled at any time with R = "1" then the FB is reset to the basic state. Please regard that data, which the CP still has received from the CPU, were sent to the communication partner.

If the R input is statically showing the signal state "1", this means that sending is deactivated.



## Note!

A minimum pulse time is necessary for a signal change to be identified. Significant time periods are the CPU cycle time, the updating time on the CP and the response time of the communication partner. Error indicationThe DONE output shows "request completed without errors". If there was<br/>an ERROR, the corresponding event number is displayed in the STATUS.<br/>If no error occurs the value of STATUS is "0".DONE and ERROR / STATUS are also output in response to a RESET of<br/>the FB. In the event of an error, the binary result BR is reset. If the block is<br/>terminated without errors, the binary result has the status "1".Please regard the parameter DONE, ERROR and STATUS are only<br/>available at one block call. For further evaluation these should be copied to<br/>a free data area.

AddressingWith LADDR the address of the corresponding CP is specified. This is the<br/>address, which was specified during hardware configuration by means of<br/>the properties of the respective interface of the CP.<br/>To access the COM2 interface you have to add 16 to the respective<br/>address value.Please regard for each interface of the CP one address is used for input<br/>and output.

Data areaThe FB 8 - P\_SND\_RK deals with an Instanz-DB I\_SND\_RK. The DB no. is<br/>transmitted with the call.It is not allowed to access the data of an instance DB.

# Firmware update

**Overview** There is the possibility to execute a firmware update of the CP 341 among others via the SPPED7 CPU by means of a MMC.

So a firmware file may be recognized and assigned with startup, a pkg file name is reserved for each updateable component and hardware release. This file name begins with "px" and differs in a number with six digits.

The pkg file name may be found at a label right down the front flap of the module.

Latest firmware at www.vipa.de The latest firmware versions may be found in the service area at www.vipa.de. For example the following file is necessary for the firmware update of the CP 341 with hardware release 1: Px000104\_V....zip



## Attention!

When installing a new firmware you have to be extremely careful. Under certain circumstances you may destroy the CP, for example if the voltage supply is interrupted during transfer or if the firmware file is defective.

In this case, please call the VIPA-Hotline!

Please regard that the version of the update firmware has to be different from the existing firmware otherwise no update is executed.

Display the Firmware version of the SPEED7 system via Web Site	The CPU has an integrated website that monitors information about firmware version of the SPEED7 components. The Ethernet PG/OP channel provides the access to this web site. To activate the PG/OP channel you have to enter according IP parameters. This can be made in Siemens SIMATIC manager either by a hardware configuration, loaded by MMC respectively MPI or via Ethernet by means of the MAC address with <b>PLC</b> > <i>Assign Ethernet Address</i> . After that you may access the PG/OP channel with a web browser via the IP address of the project engineering. More detailed information may be
	IP address of the project engineering. More detailed information may be found in the CPU manual at "Access to Ethernet PG/OP channel and website".

Load firmware and transfer it to MMC
Go to www.vipa.de.
Click on Service > Download > Firmware Updates.

- Click on "Firmware for System 300S"
- Choose the according CP modules and download the firmware Px.....zip to your PC.
- Extract the zip-file and copy the extracted file to your MMC. Following this approach, transfer all wanted firmware files to your MMC.



### Attention!

With a firmware update an overall reset is automatically executed. If your program is only available in the load memory of the CPU it is deleted! Save your program before executing a firmware update!

Transfer firmware from MMC to the CP

- 1. Get the RUN-STOP lever of your CPU in position STOP. Turn off the voltage supply. Plug the MMC with the firmware files into the CPU. Please take care of the correct plug-in direction of the MMC. Turn on the voltage supply.
- 2. After a short boot-up time, the alternate blinking of the CPU-LEDs SF and FRCE shows that at least a more current firmware file was found on the MMC.
- 3. You start the transfer of the firmware to the CP as soon as you tip the RUN/STOP lever downwards to MRES within 10s.
- 4. During the update process, the CP LEDs Rx, Tx and RUN are on.
- 5. The update is successful finished when the LEDs PWR, STOP, SF, FRCE and MCC of the CPU get on. If they are blinking fast, an error has occurred.
- 6. Turn Power OFF and ON. Now your CP is ready for operation.

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## Note!

More about firmware update may be found in the manual of the SPEED7 CPU at chapter "Deployment CPU ..." at "Firmware update".

# Chapter 5 Communication protocols

Overview In this chapter the communication protocols are described, which are supported by the CP. Here you may find the protocol specific parameters and if necessary the functionality of the corresponding protocol.

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# Overview

Serial transfer of a character	The simplest type of information exchange between two stations is the point-to-point link. Here the CP serves as interface for the CPU and a communication station. The data are serially transferred. During the serial data transfer the individual bits of one byte of an information are transferred after another in a fixed order.
Character frame	At bi-directional data transfer it is differentiated between <i>full duplex</i> and <i>half duplex</i> operation. At <i>half duplex</i> operation at one time data may be sent or received. A simultaneous data exchange is only possible at <i>full duplex</i> operation. Each character to be transferred is preceded by a synchronizing pulse as <i>start bit</i> . The end of the transferred character is formed by the <i>stop bit</i> . Beside the start and stop bit there are further parameterizable agreements between the communication partners necessary for serial data transfer. This character frame consists of the following elements:
	Speed (Baudrate)
	Character and acknowledgement delay time
	Parity
	Number of data bits
	Number of stop bits

# **Protocols** The CP serves for an automatic serial data transfer. To do this the CP is equipped with a driver for the ASCII and STX/ETX protocol. Driver for further protocols are under construction.

# ASCII

**Mode of operation** ASCII data communication is one of the simple forms of data exchange that may be compared to a multicast/broadcast function.

Individual messages are separated by means of character delay time (ZVZ). Within this time the transmitter must have sent its telegram to the receiver. A telegram is only passed on to the CPU if this was received completely.

The receiving station must acknowledge the receipt of the message within the "time delay after command" (ZNA) or command window that was defined in the sending station.

These time stamps may be used to establish a simple serial communication link.

Since during ASCII transmission apart from the usage of the parity bit no further step takes place for data protection, the data transfer is very efficiently however not secured. With the parity the inversion of one bit within a character may be secured. If two or more bits of a character are inverted, this error may no longer be detected.

**Proceeding** For the deployment of the ASCII protocol you have to add to your master system a SPEED-Bus slave and to configure a CP 341-2CH71(ASCII) as described at "Hardware configuration".

The properties dialog of the CP may be opened by a double-click. Every parameter of the ASCII protocol may be accessed via the register *Parameter Assignment* with *Device-specific parameters*.

Related to the interface the interface number COM1 respectively COM2 is put in front of the parameter designation.

## **ASCII** parameters

Transmission rateHere the transfer speed in bit/s may be selected from a selection list.<br/>Range of values: 150 ... 115200<br/>Default: 9600ProtocolLeave this value preset to "ASCII". If "No protocol" is set, the interface is<br/>deactivated and on a send job you will get an according error message.<br/>Range of values: No protocol, ASCII

Default: ASCII

Data bitsNumber of bits onto which a character is mapped.Range of values: 5 ... 8Default: 8

Parity	The addition of its value "0" or "1" brings the value of all the bits (data bits and parity bit) up to a defined status.
	Range of values: none, odd, even
	Default: none
Stop bit	When data is transmitted, stop bits are appended to each character to be sent in order to signal the end of a character.
	Range of values: 1, 2
	Default: 1
-	

**Flux control** Data flux control synchronizes data transmission when one communication partner works faster than the other. Here the type of data flux control may be set.

Value	Description
none	The flux control is deactivated.
hardware	Hardware flux control employs the RTS and CTS lines and these must therefore be wired accordingly.
XON/XOFF	Software flux control employs the control characters XON=11h and XOFF=13h. Please remember that your data must not contain these control characters.
	Range of values: none, hardware, XON/XOFF Default: none
Time after order	The delay time that must expire before a command is executed. The ZNA is to be specified in ms. Range of values: 0 65535 Default: 0
Character delay time	The character delay time defines the maximum time that may expire between two characters of a single message during the reception of the message. The ZVZ is to be specified in ms. When the ZVZ=0 the character delay time (ZVZ) will be calculated automatically (about double character time). Range of values: 0 65535 Default: 200
Number receive buffers	Defines the number of receive buffers. When only 1 receive buffer is available no more data may be received while the receive buffer is occupied. The received data may be redirected into an unused receive buffer when you chain up to a maximum of 250 receive buffers. Range of values: 1 250 Default: 1

**Setting of receive channel** For a connection with minimum reflections and the break evaluation at RS422/485 operation, the lines may be preset with defined static voltage levels. At the CP interface the wiring of the receiver is realized as follows:

Value	Description	Wiring of the receiver
None	No preassignment of the receiving lines. This setting only makes sense with bus- capable special drivers.	R(B) + R(A) -
Signal R(A) 5Volt (Break evaluation) Signal R(B) 0Volt	With this preassignment break detection is possible at full-duplex operation (RS422).	0V R(B) + R(A) - 5V
Signal R(A) 0Volt Signal R(B) 5Volt	This preassignment corresponds to the idle state (no sender is activated) at half-duplex operation with RS485. Wire-break recognition is not possible, here.	5V R(B) + R(A) - 0V

Range of values: none, R(A) 5Volt R(B) 0Volt, R(A) 0Volt R(B) 5Volt Default: none

**Operating mode** Via the operating mode you may specify if the interface is operated in half-(RS485) or full-duplex (RS422) operation.

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## Note!

At half-duplex parameterization with RS485 software data flow control is not possible.

Value	Description
full-duplex	Four-wire operation (RS422)
	Data is exchanged between the communication partners in both directions simultaneously. In full-duplex operation, therefore, data may be sent and received at the same time. Each communication partner must be able to operate a send and a receive facility simultaneously.
half-duplex	Two-wire operation (RS485)
	Data is exchanged between the communication partners but only in one direction at a time. In half-duplex operation, therefore, at any one time data is being either sent or received.

Range of values: full-duplex, half-duplex Default: full-duplex

# STX/ETX

Mode of operation STX/ETX is a simple protocol employing headers and trailers. The STX/ETX procedure is suitable for the transfer of ASCII characters (20h...7Fh). It does not use block checks. Any data transferred from the periphery must be preceded by an STX (Start of Text) followed by the data characters. An ETX (End of Text) must be inserted as the terminating character.

> The effective data, which includes all the characters between STX and ETX, are transferred to the CPU when the ETX has been received.

> When data is sent from the CPU to a peripheral device, any user data is handed to the CP where it is enclosed with an STX start character and an ETX termination character and transferred to the communication partner.

Message structure:



You may define up to 2 start and end characters. It is also possible to specify a ZNA for the sending station.

For the deployment of the STX/ETX protocol you have to add to your Proceeding master system a SPEED-Bus slave and to configure a CP 341-2CH71(STX/ETX) as described at "Hardware configuration".

> The properties dialog of the CP may be opened by a double-click. Every parameter of the STX/ETX protocol may be accessed via the register Parameter Assignment with Device-specific parameters.

> Related to the interface the interface number COM1 respectively COM2 is put in front of the parameter designation.

STX/ETX parameters	
Transmission rate	Here the transfer speed in bit/s may be selected from a selection list. Range of values: 150 115200 Default: 9600
Protocol	Leave this value preset to "STX/ETX". If "No protocol" is set, the int

reset to "STX/ETX". If "No protocol" is set, the interface is deactivated and on a send job you will get an according error message. Range of values: No protocol, STX/ETX Default: ASCII

Data bits	Number of bits onto which a character is mapped.
	Default: 8
Parity	The addition of its value "0" or "1" brings the value of all the bits (data bits and parity bit) up to a defined status.
	Range of values: none, odd, even
	Default: none
Stop bit	When data is transmitted, stop bits are appended to each character to be sent in order to signal the end of a character.
	Range of values: 1, 2
	Default: 1
	Date flux control symphronized date transmission when one communication

**Flux control** Data flux control synchronizes data transmission when one communication partner works faster than the other. Here the type of data flux control may be set.

Value	Description
none	The flux control is deactivated.
hardware	Hardware flux control employs the RTS and CTS lines and these must therefore be wired accordingly.
XON/XOFF	Software flux control employs the control characters XON=11h and XOFF=13h. Please remember that your data must not contain these control characters.

Range of values: none, hardware, XON/XOFF Default: none

- Time after orderThe delay time that must expire before a command is executed. The ZNA<br/>is to be specified in ms.<br/>Range of values: 0 ... 65535<br/>Default: 0
- Timeout (TMO)TMO defines the maximum time between two messages. TMO is to be<br/>specified in ms.<br/>Range of values: 0 ... 65535<br/>Default: 200
- Number start<br/>identificationsYou may select 1 or 2 start identifications. When you select "1" as number<br/>of start identifications, the contents of the 2. start identification is ignored.<br/>Range of values: 0 ... 2<br/>Default: 2

Start identification 1 and 2	The ASCII value of the start character that precedes a message to signify the start of a data transfer. You may select 1 or 2 start characters. When you are using 2 start characters you have to specify "2" at <i>Number of start</i> <i>identifications</i> .
	Range of values: 0 255
	Default: Start identification 1: 0, Start identification 2: 0
Number end identifications	You may select 1 or 2 end identifications. When you select "1" as number of end identifications, the contents of the 2. end identification is ignored. Range of values: 0 2 Default: 1
End identification 1 and 2	The ASCII value of the end character that follows a message to signify the end of the data transfer. You may specify 1 or 2 end characters. When you are using 2 end characters you have to enter a "2" at <i>Number of end flags</i> . Range of values: 0 255 Default: End flag 1: 3, End flag 2: 0
Setting of receive channel	For a connection with minimum reflections and the break evaluation at RS422/485 operation, the lines may be preset with defined static voltage levels. At the CP interface the wiring of the receiver is realized as follows:

Value	Description	Wiring of the receiver
None	No preassignment of the receiving lines. This setting only makes sense with bus- capable special drivers.	R(B) + R(A) -
Signal R(A) 5Volt (Break evaluation) Signal R(B) 0Volt	With this preassignment break detection is possible at full-duplex operation (RS422).	0V R(B) + R(A) - 5V
Signal R(A) 0Volt Signal R(B) 5Volt	This preassignment corresponds to the idle state (no sender is activated) at half-duplex operation with RS485. Wire-break recognition is not possible, here.	5V R(B) + R(A) - 0V

Range of values: none, R(A) 5Volt R(B) 0Volt, R(A) 0Volt R(B) 5Volt Default: none

**Operating mode** Via the operating mode you may specify if the interface is operated in half-(RS485) or full-duplex (RS422) operation.



## Note!

At half-duplex parameterization with RS485 data flow control is not possible.

Value	Description			
full-duplex	Four-wire operation (RS422)			
	Data is exchanged between the communication partners in both directions simultaneously. In full-duplex operation, therefore, data may be sent and received at the same time. Each communication partner must be able to operate a send and a receive facility simultaneously.			
half-duplex	Two-wire operation (RS485)			
	Data is exchanged between the communication partners but only in one direction at a time. In half-duplex operation, therefore, at any one time data is being either sent or received.			

Range of values: full-duplex, half-duplex Default: full-duplex

# Chapter 6 Diagnostics and error behavior

 Overview
 In this chapter the possibilities of diagnostics and the error behavior of the CP is more described.

 Each CP part has its own diganostics buffer for about 100 diagnostics entries and these are accessible as record sets.

 The record set of the corresponding CP part may be accessed by means of the SFC 59 RD\_REC.

Content	Торіс		Seite
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	Accessing	diagnostics messages	
	Diagnostic	messages	6-5

# Accessing diagnostics messages

Overview	The diagnostics functions enable you to quickly localize any errors, which occur. The following diagnostics options are available:
	<ul> <li>Diagnostics via the CP-LEDs</li> <li>Diagnostics via diagnostic buffer of the corresponding CP</li> </ul>
Diagnostics via CP-LEDs	The CP-LEDs give you an initial overview of any internal or external error as well as interface-specific errors. More information about the LEDs and their function may be found at the chapter "Hardware description".
Diagnosis via diagnostic buffer of the CP	Each CP part has its own diagnostic buffer. There every diagnostic event of the CP is stored in the order, in which they occur. The diagnostic buffer is a ring buffer for a maximum of 100 diagnostic entries. When the diagnostic buffer is full, the oldest entry is deleted when a new entry is recorded. This means that the most recent entry is always the first.
Access to the diagnostics buffer	The diagnostics buffer of the corresponding CP may be accessed by means of the handling block SFC 59 RD_REC "Read record" with the record set 80 for COM1 respectively record set 81 for COM2. Here every CP part responses with a record set of 200byte.
Error messages	<ul> <li>The following errors may be reported:</li> <li>Hardware respectively firmware errors</li> <li>Initialization and parameterization errors</li> <li>Errors during execution of a CPU request</li> <li>Data transmission error (send and receive errors)</li> </ul>
	<b>Note!</b> The contents of the diagnostic buffer is lost in the event of a PowerOFF.

## Note!

**SFC 59 - RD\_REC** The diagnostics data of the corresponding CP may be accessed by the SFC 59 RD\_REC.

The read operation is started when input parameter *REQ* is set to 1 when the call to SFC 59 is issued. The output parameter *BUSY* returns a value of 0 if the read operation was executed immediately. During read access *BUSY* returns 1. To access the diagnostics data with *LADDR* the peripheral address of the CP is specified.

The corresponding CP part is specified by *RECNUM*. Here the record set 80h stands for COM1 and 81h for COM2.

Parameter *RECORD* determines the target area. To access each diagnostics of one CP part the target area should have a length of 200byte.

## Parameters

Parameter	Declaration	Data type	Memory block	Description
REQ	INPUT	BOOL	I,Q,M,D,L, constant	REQ = 1: read request
IOID	INPUT	BYTE	I,Q,M,D,L, constant	Identifier for the address space: Because of the identical addresses for inputs and outputs here 54h should be entered.
LADDR	INPUT	WORD	I,Q,M,D,L, constant	Logical base address of the module.
RECNUM	INPUT	BYTE	I,Q,M,D,L, constant	Record set number 80h: Diagnostics data 80h 81h: Diagnostics data 81h
RET_VAL	OUTPUT	INT	I,Q,M,D,L	The return value contains an error code if an error is detected when the function is being processed. Additionally: the length of the actual record that was read, in bytes (range: +1 to +200), provided that the target area is greater than the transferred record and that no communication errors have occurred.
BUSY	OUTPUT	BOOL	I,Q,M,D,L	<i>BUSY</i> = 1: the write operation has not been completed.
RECORD	OUTPUT	ANY	I,Q,M,D,L	Target area for the record that was read. To access the whole 100 diagnostics the area should have a length of 200byte. When SFC 59 is processed in asyn- chronous mode you must ensure that the actual parameters of <i>RECORD</i> have the same length information for all calls. Only data type BYTE is permitted.

Suitable choice of RECORD	To ensure that an entire record of one CP part is read, you must select a target area with a length of 200byte. In this case the value in <i>RET_VAL</i> indicates the actual length of the data that was transferred successfully.
RET_VAL (Return value)	<ul> <li><i>RET_VAL</i> contains an error code when an error occurs while the function was being processed.</li> <li>When the transfer was successful <i>RET_VAL</i> contains:</li> <li>a value of 0 if the entire target area was filled with data from the selected record (the record may, however, be incomplete).</li> <li>the length of the record that was transferred, in bytes (valid range: 1 to 200), provided that the target area is greater than the transferred record</li> </ul>
Error information	<ul> <li>Two distinct cases exist for RET_VAL = 8xxxh:</li> <li>Temporary error (error codes 80A4h, 80Cxh): For this type of error it is possible that the error corrects itself without intervention. For this reason it is recommended that you re-issue the call to the SFC (once or more than once). Example for temporary errors: the required resources are occupied at present (80C3h).</li> <li>Permanent error (error codes 809xh, 80A0h, 80Bxh):</li> </ul>
	These errors cannot be corrected without intervention. A repeat of the call to the SFC is only meaningful when the error has been removed. Example for permanent errors: incorrect length of the record that must be transferred (80B1h).

Value	Description
7000h	First call with REQ = 0: data transfer not active; BUSY is set to 0.
7001h	First call with REQ = 1: data transfer initiated; BUSY is set to 1.
7002h	Intermediate call (REQ irrelevant): data transfer active; BUSY is set to 1.
8090h	The specified logical base address is invalid: no assignment available in
	SDB1/SDB2x, or this is not a base address.
8092h	ANY-reference contains a type definition that is not equal to BYTE.
8093h	This SFC is not valid for the module selected by LADDR and IOID.
80A0h	Negative acknowledgement when reading from the module (module was
	removed during the transfer or module failed).
80A4h	Communication failure (this fault occurs between the CPU and the
	external DP interface).
80B0h	SFC not valid for the type of module.
	Module does not recognize the record.
	<ul> <li>Record number ≥ 241 not permitted.</li> </ul>
80B1h	The length specified in parameter RECORD is wrong.
80B2h	The slot that was configured has not been populated.
80C3h	Required resources (memory, etc.) are currently occupied.
80C4h	Communication error

# **Diagnostic messages**

Structure

Each diagnostics message has a length of 2byte and the following structure:

Bit	15 13	12		8	7		0
	reserved	Event	class			Event number (Error number)	

0000h indicates no diagnostics entry is available.

Event classes	The table below describes the various event classes and numbers:
and event	
numbers	

Event class 00h "CP star	t-up"		
Event class / number	Description		
00 03h	PtP parameter accepted		
00 04h	Parameter already on CP (timers match)		
00 07h	Status transition CPU to STOP		
00 08h	Status transition CPU to RUN/START-UP		
Event class 01h "Hardwa	are fault on CP"		
01 01h	Fault while testing operating system EPROM of CP		
	Remedy: CP defective and must be replaced.		
01 02h	RAM test of CP faulty		
	Remedy: CP defective and must be replaced.		
01 03h	Request interface of CP defective		
	Remedy: CP defective and must be replaced.		
01 10h	Fault in CP firmware		
	Remedy: Switch CP off and on again. If necessary, replace CP.		
Event class 02h "Initializa	ation error"		
02 0Fh	Invalid parameterization detected at start of parameterized communication. Interface could not be parameterized.		
	Remedy: Correct the non-permissible parameterization and initialize a start-up.		
Event class 03h "Error parameterization of FBs"			
(not displayed in diagnostic buffer)			
03 01h	Invalid or no source/destination data type Invalid area (start address, length) DB invalid or no DB (e.g. DB 0) or other data type invalid or missing. <i>Remedy: Check parameterization on CPU and CP and correct if</i> <i>necessary.</i>		

continue ...

## ... continued

Event class 04h "CP detected error in data traffic CP - CPU"		
04 03h	Incorrect, unknown or illegal data type	
	(e.g. wrong parameterization of FB)	
04.071	Remedy: Check program for incorrect parameterization of the FB.	
04 07h	Error during data transmission between CPU and CP.	
	have called in user program are parameterized correctly.	
	If error is indicated immediately after PowerON, no connection has yet been set up to the CPU. In the case of the ASCII driver, the receiving CP re-attempts data transfer until the data is transmitted to the CPU.	
	If fault indication is sporadic in the course of data transfer, the CPU is temporarily unable to accept data. In the case of the ASCII driver the receiving CP re-attempts data transfer until the data is transmitted to the CPU.	
04 08h	Error during data transmission between CPU and CP (reception).	
	CPU is temporarily overloaded, request queued for repetition.	
	Remedy: Reduce number of communication calls	
	CPU data area temporarily unavailable for access, for example because receive block is called too infrequently.	
	Remedy: Call the receive block more frequently.	
	• CPU data area temporarily unavailable for access, for example because receive block is temporarily locked (EN = false).	
	Remedy: Check whether the receive block is disabled for too long.	
Event class 04h "CP c	letected error in data traffic CP - CPU"	
04 09h	Data cannot be received. Error during data transmission between CPU and CP (reception). Request is canceled in 10s following multiple attempts, because:	
	Receive block is not called	
	Remedy: Check whether your user program runs the receive block.	
	Receive block is disabled	
	Remedy: Check whether the receive block is disabled.	
	Access to CPU data area denied	
	Remedy: check that the data area to which the data is to be transferred is available.	
	CPU data area too short.	
	Remedy: Check the length of the data area.	
04 0Ah	Error during data transmission between CPU and CP. Data transfer canceled by RESET because:	
	Destination DB is not available	
	Destination DB is too short	
	RESET bit set at FB.	
	Remedy: Create destination DB in the user program or increase the length of the existing destination DB, as applicable.	

continue ...

## ... continued

Event class 05h "error while processing CPU request"		
05 01h	Current request aborted as a result of CP restart. Remedy: No remedy is possible at PowerON. When re-parameteriza-	
	tion of the CP from the programming device, before writing an interface you should ensure there are no more request running from the CPU.	
05 02h	Request not permitted in this operating mode of CP	
	Remedy: Parameterize the device interface.	
05 14h	Specified start addresses too high for desired data type, or start address or DB/DX number too low.	
	Remedy: Obtain from the request tables the permissible start addresses and DB/DX numbers that can be specified in the program.	
05 17h	Transmission length > 1kbyte too great for CP or too short for interface parameter.	
	Remedy: Split the request up into several shorter requests.	
Event class 07h "Send e	rror"	
07 08h	The waiting time for XON respectively CTS = ON has elapsed.	
	Remedy: The communication partner has a fault, is too slow or is	
	switched off-line. Check the communication partner or, if necessary, change the parameterization	
Event class 08h "Receive error"		
08 0Ah	There is no free input buffer available.	
	Remedy: The FB P_RCV_RK must be called more frequently.	
08 0Bh	Internal input buffer is full.	
	Remedy: The FB P_RCV_RK must be called more frequently.	
08 0Ch	Transmission error:	
	<ul> <li>Transmission error (parity error-, stop bit error or overflow error) detected.</li> </ul>	
	Remedy: Disturbances on the transmission line cause message frame	
	repetitions, thus lowering user data throughput. Danger of an	
	line installation. Check connecting cable of communications partner or	
	check whether both devices have same setting for baud rate, parity and number of stop bits.	
08 0Dh	BREAK	
	Receive line to partner is interrupted.	
	Remedy: reconnect or switch partner on again. Check and change the connector pin assignment of the 2-wire receiving line R(A), R(B).	

continue ...

## ... continued

Event class 08h "Receive error"		
08 10h	Parity error	
	Remedy: Check the connecting cables of the communication partners or check whether both devices have the same setting for baud rate, parity and number of stop bits.	
08 11h	Character frame error	
	Remedy: Check the connecting cables of the communication partners or check whether both devices have the same setting for baud rate, parity and number of stop bits.	
	Change your system setup or cable wiring.	
08 15h	Discrepancy between settings for transfer attempts at CP a commu- nication partner.	
	Remedy: Parameterize same number of transfer attempts at	
	communication partner as at CP. Check for malfunction at partner	
	device, possible by using interface test device switched into the transmission line.	
08 16h	• The length of a received message frame was longer than the length agreed upon.	
	Remedy: a correction is necessary at the partner.	
	<ul> <li>The length of the parameterized input buffer is too short.</li> </ul>	
	Remedy: the length of the input buffer must be enlarged.	
Event class 30 (1Eh) "Error during communication between CP and CPU via backplane bus"		
1E 0Dh	Request aborted due to complete Restart or Reset.	

# Appendix

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